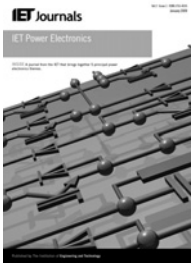
Published in IET Power Electronics
Received on 4th August 2008
Revised on 12th November 2008
doi: 10.1049/iet-pel.2008.0253



ISSN 1755-4535

A DC–DC multilevel boost converter

J.C. Rosas-Caro[1] *J.M. Ramirez*[1] *F.Z. Peng*[2] *A. Valderrabano*[1]

[1]*Cinvestav – Unidad Guadalajara, Av. Cientifica 1145, Colonia El Bajio, Zapopan, Jalisco 45015, Mexico*
[2]*Michigan State University, East Lansing, MI, USA*
E-mail: jramirez@gdl.cinvestav.mx

Abstract: A DC–DC converter topology is proposed. The DC–DC multilevel boost converter (MBC) is a pulse-width modulation (PWM)-based DC–DC converter, which combines the boost converter and the switched capacitor function to provide different output voltages and a self-balanced voltage using only one driven switch, one inductor, $2N - 1$ diodes and $2N - 1$ capacitors for an Nx MBC. It is proposed to be used as DC link in applications where several controlled voltage levels are required with self-balancing and unidirectional current flow, such as photovoltaic (PV) or fuel cell generation systems with multilevel inverters; each device blocks only one voltage level, achieving high-voltage converters with low-voltage devices. The major advantages of this topology are: a continuous input current, a large conversion ratio without extreme duty cycle and without transformer, which allow high switching frequency. It can be built in a modular way and more levels can be added without modifying the main circuit. The proposed converter is simulated and prototyped; experimental results prove the proposition's principle.

1 Introduction

The transmission and distribution power systems have the natural trend to increase the voltage rating which increase the efficiency, whereas microelectronics and digital systems have the natural trend to decrease the voltage rating to reduce size, increase the efficiency and the speed of digital systems. Such scenario represents interesting challenges in buck-based power supply developments because of the extremely low-voltage gain; the conventional buck converter sacrifice the switching frequency and the system size because of the extremely low duty cycle or the transformer requirement [1–3]. A good example of this is the computers' power supply where a microprocessor needs to be fed with less than 3 V DC and the power supply is fed with 110 V/220 V AC.

On the other hand, for the boost converter supplies analogue challenges are emerging. There are applications where high voltage and low current are needed such as TVCRTs, lasers, X-ray systems, ion pumps and electrostatic systems [4]. Likewise, applications in renewable energy generation systems where the low voltage of a photovoltaic (PV) panel or a fuel cell necessitates being boosted in order to feed a grid connected inverter that can push the power into the grid. For telecom standard equipment for providing internet services, the 48 V of the DC battery plant has to be boosted to a 380-V intermediate DC bus [3]. The high-intensity discharge (HID) lamps for automobile head lamps during their start-up require the voltage increment from the battery's 12 V to more than 100 V at 35 W [3].

A transformer with a large voltage gain is undesirable because it enhances the transformer non-idealities [4]. To reduce the DC–DC converters' size, the use of high switching frequency results in small inductors and capacitors with an equivalent current and voltage ripple [1–4]. This is the motivation to use several hundreds of kilohertz [1]. The natural switching delays in actual switches limit the switching frequency when the duty ratio is too small; a solution to this is the employment of transformers to reduce the voltage without using small duty ratios. However, the transformer's losses limit the switching frequency also; along with the development of high-speed MOSFETs the switching frequency limitation becomes a transformer's issue [1–4].

In the buck-type power supply, several topologies have been proposed to avoid the above-mentioned limitations [1–3], achieving extremely low-voltage gains without extremely low duty cycles.

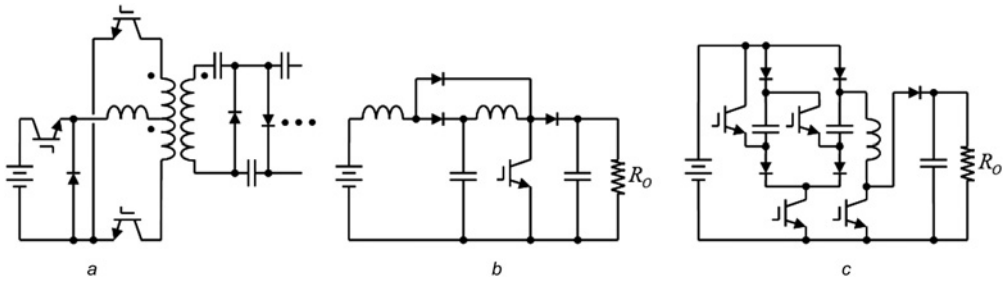


Figure 1 *Conventional DC–DC converters*

a Buck followed by a push–pull voltage multiplier
b QBC
c Switched capacitor converter with a boost stage

For the boost-type converters, there are several topologies for implementing a high-efficiency transformer-less converter with high boost ratios (all of them with relatively high complexity, compared with the conventional single switch converter). For instance, (i) Fig. 1*a* illustrates a DC–DC high-voltage converter with a buck converter followed by a push–pull voltage multiplier. It may be extended to high-voltage applications with low-voltage devices by adding capacitors and diodes, without modifying the power stage. However, it requires two stages including three switches and a complex control system; the input current is discontinuous [4]. (ii) Fig. 1*b* shows the cascade boost, also named quadratic boost converter (QBC). It may be extended to attain a higher boost ratio using only one switch. The input current is continuous. However, the switch is rated to the total output voltage, which avoids the use of high voltage. It requires several inductors, which is the bulkiest part and it is hard to encapsulate. Furthermore, novel topologies have been recently proposed to overcome the mentioned challenge; for example, (iii) in [5] (see Fig. 1*c*), a converter is proposed based on the switched capacitor, which charge N capacitors to the input voltage, and connect them in series to feed a boost stage. The switched capacitor stage can operate with high efficiency since it does not regulate the output voltage, which is regulated with the boost stage. However, it requires a high number of switches and the output switch is rated to the output voltage. All these topologies and others [1–3, 5] achieve high-voltage gain without an extremely high duty ratio and transformer-less, except (i), Fig. 1*a*, which uses a transformer.

The use of the diode clamped multilevel converters (DCMLC) for renewable energy micro generation brings the promise to build compact converters made with small power MOSFETS, with a minimum ESR connected transformer-less to the utility grid. There exists the challenge to couple the low DC voltage from the renewable energy source to the high DC-link voltage of the multilevel converter. The DCMLC needs external balance of the DC link for proper operation [6]. The former topologies have limitations for this purposes: (i) For high-voltage applications, they require high-voltage devices; this limitation leads to a novel solution in the DC–AC conversion with multilevel inverters [7, 8], where high-voltage converters can be built with low-voltage rating devices, because of each device only blocks one voltage level. Multilevel converters have been studied in DC–DC applications with the topologies: diode clamped, capacitor clamped and cascaded cells [9], and it has been shown that, excluding the diode clamped topology, they are suitable for such purposes. (ii) The second big limitation is that they cannot provide a voltage balancing for the DC link in the DCMLC; the use of an external balancing circuit is necessary [6].

The utilisation of combined boost converters with switched capacitors has been studied in [5, 10]. However, the output voltage is limited by the voltage rating devices. A topology that can be extended to high voltage is presented in [4]; the disadvantage is that the output voltage is negative with respect to the input.

With the growing of distributed generation based on PV systems, and the advent of new sources of distributed generation DC based such as fuel cells, DC–DC converters with high-voltage boost ratios are desirable to use those renewable sources in order to feed multilevel inverters and push the power into the utility for some hundreds of volts.

This paper proposes a novel DC–DC converter topology, initially introduced in [11]. The DC–DC multilevel boost converter (MBC) is a converter that combines the boost converter and the switched capacitor function to provide an output of several capacitors in series with the same voltage and self-balanced voltage, which is important for some applications such as feeding a diode clamped multilevel inverter that cannot balance the voltage by itself. It can control the voltage by pulse-width modulation (PWM) in all the output levels with only one driven switch, one inductor, $2N-1$ diodes and $2N-1$ capacitors for an Nx MBC, The number of levels can be increased by adding capacitors and diodes, then it is possible to achieve modular implementations.

doi: 10.1049/iet-pel.2008.0253

It is proposed to be used as DC link in applications where several controlled voltage levels are wanted with self-balancing and unidirectional current flow, such as PV or fuel cell generation systems with multilevel inverters. The major advantages of this topology are: (i) continuous input current and (ii) a large conversion ratio with low duty cycle and without a transformer. It can be built in a modular way and more levels can be added without changing the main circuit; it provides several self-balanced voltage levels and only one switch is necessary. The converter's principle is proven by simulation and experimental results.

2 DC–DC multilevel boost converter

Fig. 2 depicts the proposed topology. It is a *Nx* DC–DC converter based on one driven switch, $2N-1$ diodes and $2N-1$ capacitors. One advantage of the topology is that the number of levels can be extended by only adding capacitors and diodes and the main circuit does not need to be modified.

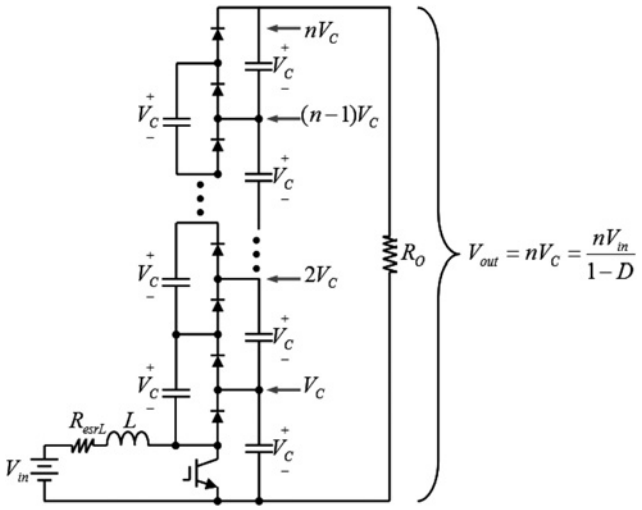


Figure 2 *DC–DC MBC for Nx or N + 1 levels*

The lowest part of the converter, Fig. 3, is the conventional DC–DC boost converter. Thus, the voltage gain holds by the well-known boost converter equations. The difference between the MBC and the conventional one is that in the MBC, the output is V_c times N, where $N+1$ is the converter's number of levels taking into account the zero level, Fig. 2. This behaviour is achieved, thanks to the voltage multiplier in the boost converter's output that is driven by the only switch in the converter.

During the switch-on state, the inductor is connected to V_{in} voltage, Fig. 3*a*. If C_6's voltage is smaller than C_7's voltage then C_7 clamps C_6's voltage through D_6 and the switch S, Fig. 3*b*. Simultaneously, if the voltage across $C_4 + C_6$ is smaller than the voltage across $C_5 + C_7$, then C_5 and C_7 clamp the voltage across C_4 and C_6 through D_4 and S, Fig. 3*c*. In a similar way, C_3, C_5 and C_7 clamp the voltage across C_2, C_4 and C_6, Fig. 3*d*.

When the switch turns off, the inductor current closes D_7, and switches all diodes. During the switch-off state, the inductor current closes D_7 charging C_7, Fig. 4*a*. When D_7 closes, C_6 and the voltage in V_{in} plus the inductor's voltage clamp the voltage across C_5 and C_7 through D_5, Fig. 4*b*. Similarly, the voltage across the inductor plus V_{in}, C_4 and C_6 clamp the voltage across C_3, C_5 and C_7 through D_3. Finally, the voltage across C_1, C_3, C_5 and C_7 is clamped by C_2, C_4, C_6, V_{in} and the inductor's voltage, Fig. 4*c*.

It is noteworthy that D_1, D_3, D_5 and D_7 switch in a synchronously way, complemented with D_2, D_4, D_6 and S, Figs. 3 and 4.

3 Effect of the equivalent series resistance (ESR) (R_{esrL}) on the boost ratio

Similarly to the conventional boost converter, and all converters with boost capability, the ideal maximum boost

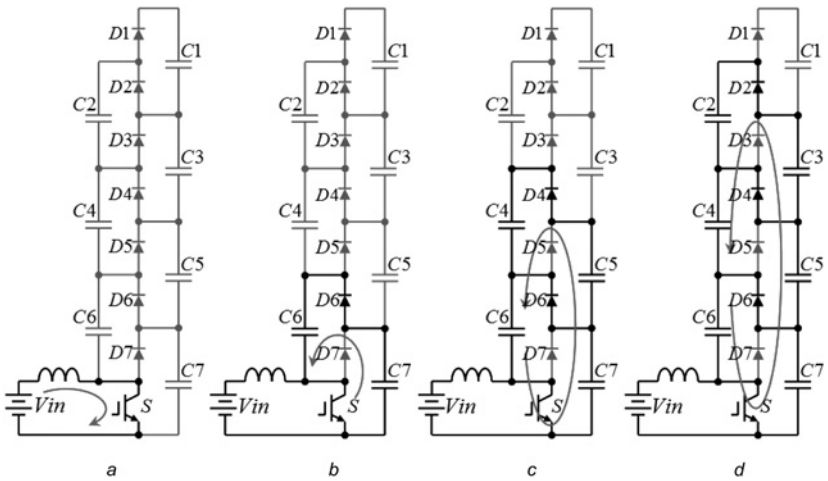


Figure 3 *Switch-on state*

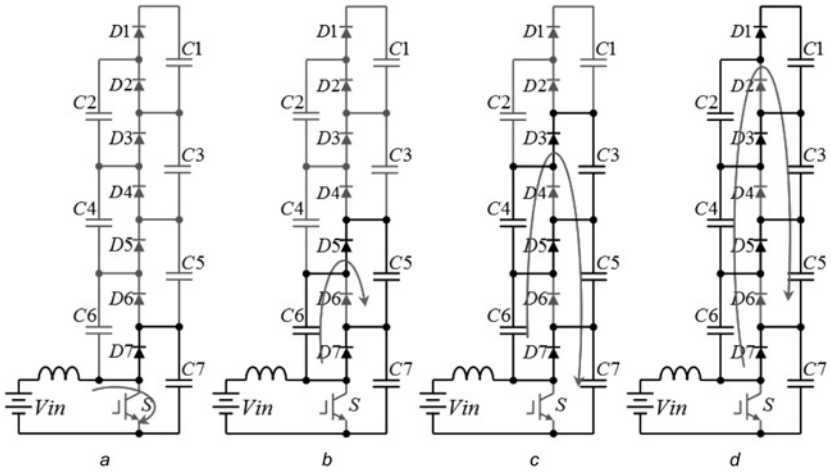


Figure 4 *Switch-off state*

ratio is infinite. In actual applications, it is limited by the parasitic resistance in the passive components; in the boost converter case the main limitation is given by the ESR in the input inductor. This effect is caused by the fact that the input current is the output current times the boost ratio.

It is important to emphasise that the use of high switching frequency allows using a smaller input inductance with a smaller ESR. This limitation, which appears in all converters with an input inductor, is also reduced in a converter designed to work with a high switching frequency.

As aforesaid, the first level is a usual boost converter which equations and behaviour are well known, but the total output voltage is N times V_C. Equations (1) and (2) express the boost ratio and the inductor current in the boost converter, Fig. 2

$$\frac{V_C}{V_{in}} = \frac{1}{1-D} \tag{1}$$

$$I_L = \frac{V_C}{(1-D)R_O} \tag{2}$$

being R_O the load resistance, considering the ideal $1x$ or conventional boost converter.

Thus, the new voltage gain can be expressed by

$$\frac{V_C}{V_{in}} = \frac{1}{1-D} \quad \text{then} \quad \frac{V_{out}}{V_{in}} = \frac{N}{1-D} \tag{3}$$

The input DC current can be expressed in terms of the output current and input–output voltage by

$$V_{in}I_L = V_{out}I_{out} = V_{out}\frac{V_{out}}{R_O} = NV_C\frac{NV_C}{R_O} = \frac{N^2V_C^2}{R_O}$$

$$I_L = \frac{V_C}{V_{in}}\frac{N^2V_C}{R_O} = \frac{N^2V_C}{(1-D)R_O} \tag{4}$$

From (4) it can be noticed that the input current can be controlled with D in the PWM, which is important in some applications such as renewable energy-based distributed generation systems, where is highly desirable to track the maximum power point by controlling the input current.

The following expressions can be derived from the first level: (1) and (2) just like the conventional boost converter. Taking into account the relationship between the capacitors voltage against the output voltage and (4), (5) can be derived by the following procedure in which the inductors power losses are considered.

The average voltage in the inductor V_L is zero at steady state, and is equal to the voltage in both switching states times the time that each switching state holds. In the continuous mode, including the inductor's ESR (R_{esrL})

$$V_L = D(V_{in} - I_L R_{esrL}) + (1-D)(V_{in} - V_C - I_L R_{esrL}) = 0$$
$$DV_{in} - DI_L R_{esrL} + (1-D)V_{in} - (1-D)V_C - (1-D)I_L R_{esrL} = 0$$
$$V_{in}(D + 1 - D) + I_L R_{esrL}(-D - 1 + D) = (1-D)V_C$$
$$V_{in} = (1-D)V_C + I_L R_{esrL}$$
$$V_{in} = (1-D)\frac{V_{out}}{N} + \frac{NV_{out}}{(1-D)R_O}R_{esrL} \tag{5}$$

From (5), the boost ratio for the novel topology may be expressed as (6)

$$\frac{V_{in}}{V_{out}} = \frac{1}{((1-D)/N) + (NR_{esrL}/(1-D)R_O)} \tag{6}$$

It is noteworthy that (6) is actually a general expression that includes the conventional boost converter if $N = 1$. In the ideal model, when $R_{esrL} = 0$ the infinite boost ratio results.

doi: 10.1049/iet-pel.2008.0253

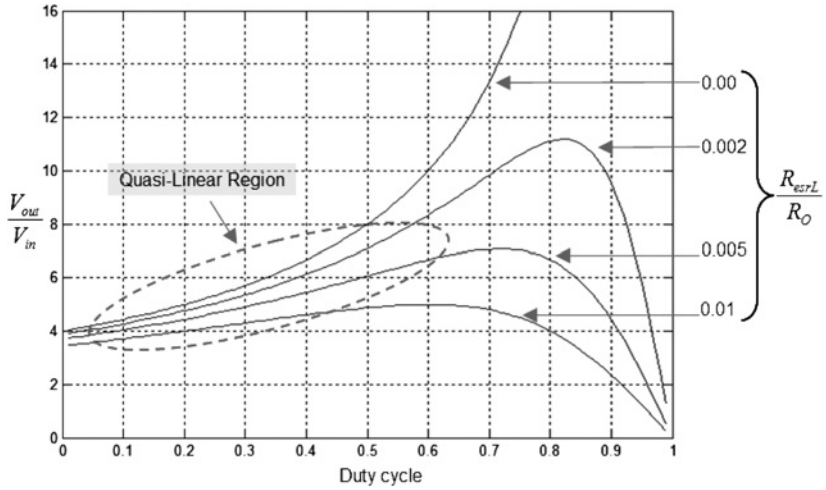


Figure 5 *Voltage gain against duty cycle for different values of ESR/R_O in the novel MBC ($N = 4$)*

Fig. 5 exhibits the case when $N = 4$ for different cases of $R_{\text{esrL}}/R_{\text{O}}$. The boost ratio is plotted against the duty cycle. It can be noticed that the graphic shows a quasi-linear region larger than the traditional boost converter, which becomes highly non-linear when the duty cycle is near 1. Thus, the MBC can operate in the high boost ratio region, this region is around $D = 0.5$ which is the best point to operate the multilevel strategy.

Likewise, the maximum boost ratio is farther than $D = 1$, which is an operative point difficult to implement with non-ideal switches.

4 Switches' and diode's voltage drop

In actual implementations the switches' and diodes' voltage drop must be taken into account since it avoids capacitors to be charged to V_{C} (the voltage in the lower capacitor); this effect is studied in the present section.

The voltage drop in conventional IGBTs and power diodes can be around 2 V (in low power is much smaller), and it can be ignored in medium- and high-voltage applications with several hundred volts, but in low-voltage applications must be considered. For simplicity, the voltage drop in switches and diodes is assumed to be equal to V_{d}. From the circuit in Figs. 3 and 4, in Fig. 6 can be noticed that the actual voltage across C_6 becomes

$$\begin{aligned} V_{C6} &= V_{C7} - V_{\text{switch}} - V_{\text{Diode}} \\ V_{C6} &= V_{C7} - 2V_{\text{d}} \end{aligned} \tag{7}$$

Observe that

$$V_{C5} = V_{C7} - 4V_{\text{d}} \tag{8}$$

It is worth noting that the current charging C_5 does not go across D_7, it actually goes across the input inductor and the input voltage source, but D_7 is closed during D_5 is closed as it is above mentioned, then the voltage across C_5 can be expressed as (8). In Fig. 7, it can be seen that the voltage across C_7 and C_5 clamps the voltage across C_6 and C_4 with two diodes voltage drop. The voltage drop in the voltage multiplier does not depend on the level after the second level, and all capacitors after the second level are charged to $V_{C7} - 4V_{\text{d}}$.

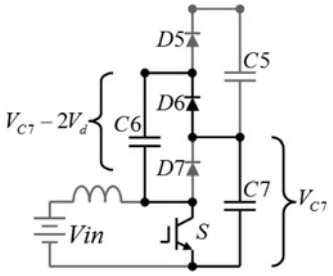


Figure 6 *Charging C_6 with diode's and switch's voltage drop*

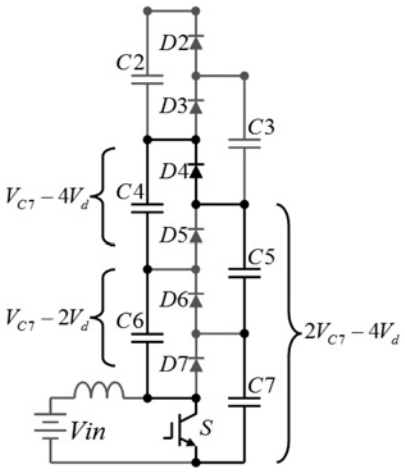


Figure 7 *Charging C_4 with diode's and switch's voltage drop*

The expression of the output voltage for the circuit in Figs. 3 and 4 can be obtained as (4*x* converter)

$$V_{\text{out}} = 4V_{C7} - 12V_{\text{d}} \tag{9}$$

Finally, the output voltage general expression in an *Nx* MBC is (10). This one must be considered to design a multilevel voltage multiplier

$$V_{\text{out}} = NV_{\text{C}} - (N-1)4V_{\text{d}} \tag{10}$$

where V_{C} is the voltage of the lower capacitor, and follows the traditional boost converter equation. The efficiency of the switched capacitor multiplier stage is given by (11) as in all step-up switched capacitor converters [12]

$$\eta = \frac{V_{\text{out}}}{NV_{\text{C}}} = \frac{NV_{\text{C}} - (N-1)4V_{\text{d}}}{NV_{\text{C}}} = 1 - \frac{(N-1)4V_{\text{d}}}{NV_{\text{C}}} \tag{11}$$

From (11) it can be seen that the converter is ideal for application with several hundred volts where V_{d} is negligible compared with V_{C}; the power losses in the switch can be calculated as in the traditional boost converter. It is important to notice that the switching losses are proportional to the voltage that the switch has to block which is reduced in this topology compared with other solutions.

5 Central source

A variation of the proposed topology is discussed in this section. As a natural extension of the voltage multiplier the negative part of the output voltage can be added and then the converter shown in Fig. 8 can be realised. One of the disadvantages of the proposed topology, Fig. 2, is that the current in semiconductors is higher in the lower levels. This is a disadvantage for many of the DC–DC multilevel converters. For instance, if a capacitor clamped multilevel converter is used as a DC–DC converter the lower device would dissipate more power than the higher one. By utilising the medium source variation, this disadvantage can be reduced.

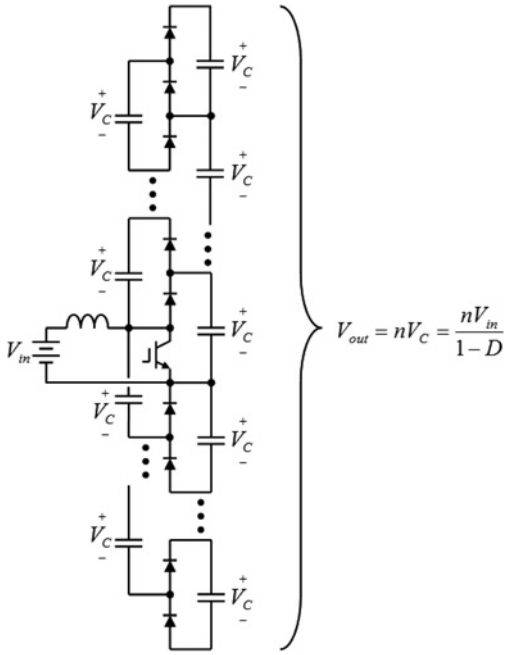


Figure 8 *Topology variation with medium source*

Fig. 8 displays the topology variation with the input source voltage at the medium position. Similarly to Fig. 2, the topology can be easily extended to any number of levels by adding diodes and capacitors.

It is noteworthy that the multilevel operation holds and the capacitor's voltage are balanced, regardless on the load and configuration, non-medium, or a medium source. Thus, the DC–DC MBC is an important alternative to feed multilevel inverters.

6 Design and discussion

The output voltage will have a small ripple which can be minimised to a desired value by selecting correct values for the capacitors, a design analysis is done with a 2*x* MBC, Figs. 9*a* and 9*b* show the possible switching states, Fig. 9*c* shows a zoom in the voltage ripple of the capacitors V_1 is the voltage across c_1 and so on, the duty cycle is 0.5, starting the analysis when the switch is open c_2 just transferred energy to c_3, and c_1 has been charging during the last half a cycle, c_1 has a higher voltage than c_2, right after the switch closes c_1 charges c_2 through d_2 and they get the same voltage expressed as

$$V_{1\text{ac}} = V_{2\text{ac}} = \frac{V_{1\text{bc}}c_1 + V_{2\text{bc}}c_2}{c_1 + c_2} \tag{12}$$

Where $V_{1\text{ac}}$ is V_1 after closing the switch, $V_{1\text{bc}}$ is V_1 before closing the switch and so on. After this happen c_2 does not transfer energy to the load and its voltage keeps constant during all the next half a cycle, c_1 and c_3 get a voltage drop because the are feeding the load, this voltage drop is Δ_{v1} in Fig. 9*c* and can be expressed as (assuming all capacitors have the same capacitance)

$$\Delta_{v1} = \Delta_{v12} = \frac{1}{c_1} I_{\text{out}} \Delta_{t1} = \frac{1}{c_2} I_{\text{out}} \Delta_{t1} \tag{13}$$

During Δ_{t1}, c_1 and c_3 in series feed the load, and c_2 just store charge to be transferred to c_3 during Δ_{t3}, the time when the switch is open Δ_{t2} can be divided into two, Δ_{t3} and Δ_{t4}, right after the switch opens c_2 has a voltage higher than c_3 and c_2 discharges whereas c_3 charges until they get the same voltage, the voltage drop in c_2 can be expressed as

$$\Delta_{v4} = \frac{1}{c_2} I_{\text{L}} \Delta_{t3} \tag{14}$$

doi: 10.1049/iet-pel.2008.0253

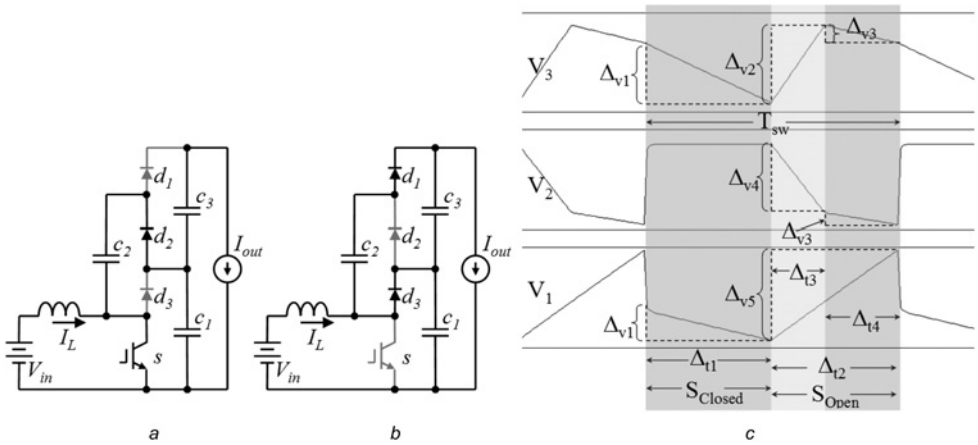


Figure 9 *2x MBC*

a Switch-on state
b Switch-off state
c Voltage ripple in capacitors

And the ripple Δ_{v2} in c_3 can be expressed as

$$\Delta_{v4} = \frac{1}{c_2}(I_{\mathrm{L}} - I_{\mathrm{out}})\Delta_{t3} \tag{15}$$

After that, both capacitors in parallel fed the load in series with c_1; it is important to note that during Δ_{t2} c_1 keeps charging with $I_{\mathrm{L}} - I_{\mathrm{out}}$, this is clear considering the KCL in the reference node. Finally the voltage drop Δ_{v3} in c_2 and c_3 can be expressed as

$$\Delta_{v3} = \frac{1}{c_2}\left(\frac{I_{\mathrm{out}}}{2}\right)\Delta_{t4} = \frac{1}{c_3}\left(\frac{I_{\mathrm{out}}}{2}\right)\Delta_{t4} \tag{16}$$

And Δ_{v5} can be expressed as

$$\Delta_{v5} = \frac{1}{c_1}(I_{\mathrm{L}} - I_{\mathrm{out}})\Delta_{t2} = \frac{1}{c_1}(I_{\mathrm{L}} - I_{\mathrm{out}})(\Delta_{t3} + \Delta_{t4}) \tag{17}$$

The output voltage is V_1 plus V_3 then the ripple in the output voltage can be expressed as the ripple in c_1 plus the ripple in c_3, by using (12)–(17) the capacitors and switching frequency can be selected to fit the application and the input inductor can be calculated as in the traditional boost converter to fit the desired input ripple current with the first level voltage. This analysis can be extended to more levels.

Table 1 summarises a comparison between the proposed topology ($x = 2$), the QBC (Fig. 1*c*), and the switched capacitor with the boost stage (SCBS) for $n = 2$ (Fig. 1*b*).

Table 1 offers a general idea about the topological comparison, although each converter presents advantages for specific applications. Some comments about individual characteristics are as follows. The SCBS has the advantage that the switched capacitor stage only multiplies the voltage that is regulated by the boost stage, which makes possible for the switched capacitor stage to operate in high efficiency but it is the more complex in terms of number of components and control. It has two control variables (x and D). Additionally, it has the highest voltage gain when D and $x = 0.5$, which is the optimum point for working at high frequency. One more advantage is that, similarly to all switched capacitor converters, the switched capacitor stage can be encapsulated in an IC creating a small design.

The QBC is the least complex in terms of number of components, but it needs at least two inductors that are the bulkiest components. The gain is highly non-linear, which makes the controller design an important challenge. The 2*x* MBC has the lower voltage gain, but it also has the lower voltage stress in the switches and the voltage stress does not increase when more levels are added for increasing the voltage gain. A major advantage of the converter arises when feeding a DCMLC. It automatically balances the multilevel DC link. A disadvantage of such topology is that

Table 1 Comparison of topologies

Converter	Inductors	Capacitors	Switches	Diodes	Voltage gain	Switch stress
SCBS	1	3	4	5	$(3 - 2xD)/(1 - D)$	V_{out}
QBC	2	2	1	3	$1/(1 - D)^2$	V_{out}
2*x* MBC	1	3	1	3	$2/(1 - D)$	$V_{\mathrm{out}/2}$

the capacitors are used to transfer the energy in the voltage multiplier while feeding the load according to (12)–(17). This emphasises the traditional tradeoff between the output voltage ripple and the size in the capacitor selection. Again, for feeding a DCMLC the inverter control can alleviate this fact by utilising the feed-forward control, which allows having an AC output voltage free of distortion coming from the voltage ripple in the DC link.

7 Experimental results

A low-power prototype is built to experimentally show the operating principle of this novel converter. A Freescale 8-bit microcontroller is employed to provide the PWM signal in an open-loop structure with a switching frequency of 100 kHz, the duty cycle is 0.5 (measured in the IGBT terminals), the input voltage is 50V and then the output voltage is 300 V. Fig. 10 displays the prototype schematic of a 3*x* (four levels) MBC. Fig. 11 exhibits the test bench. The switch is the IGBT-12N60A4D and the fast recovery diodes are BY229X-800. The inductor has a value of 1.33 mH, and all capacitors are 100 μF–250 V (aluminium electrolytic) in parallel with 2 μF–250 V (polyester). The inductor is added externally to the PBC prototype. Several tests are carried out with resistive load. Figs. 12 depict the resultant waveforms. The results are within the expectations, with waveforms and values close to those

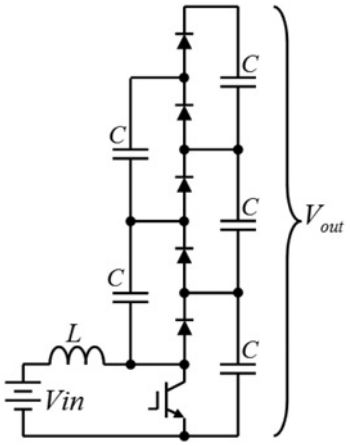


Figure 10 *Prototype schematic: L = 1.33 mH, C= 100 μF*

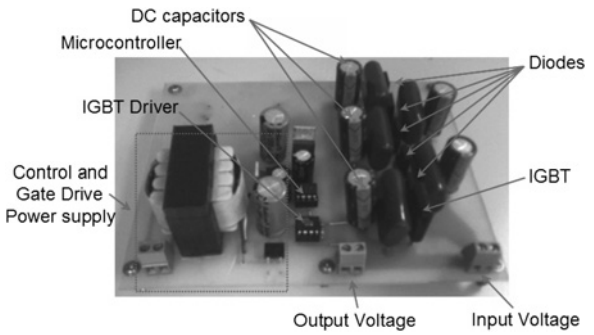


Figure 11 *3x MBC prototype*

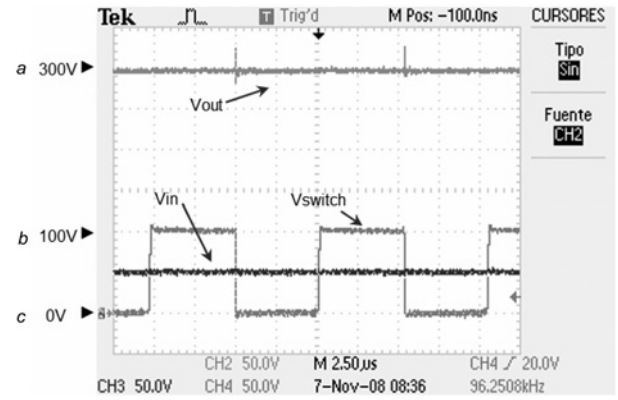


Figure 12 *Actual signals from the prototype*

a Switch voltage
b Lower capacitor voltage
c Input voltage

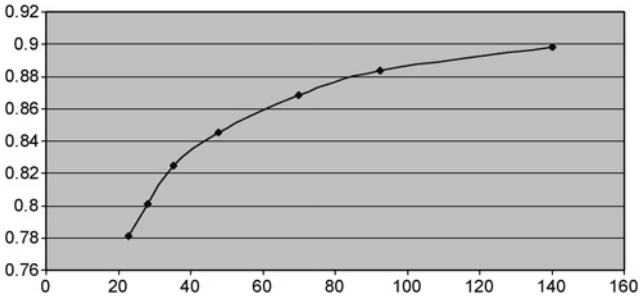


Figure 13 *Efficiency against output power*

estimated by equations and Fig. 13 shows the measured efficiency against output power.

8 Conclusions

This paper proposes a DC–DC converter topology. The DC–DC MBC is based on only one driven switch, one inductor, $2N-1$ diodes and $2N-1$ capacitors for an Nx MBC. It is proposed to be used as DC link in applications where several controlled voltage levels are needed with self-balancing and unidirectional current flow, such as PV or fuel cell generation systems with multilevel inverters.

The main advantages of this topology are:

- A continuous input current.
- A big conversion ratio without extreme duty cycle.
- Transformer-less.
- Allow high switching frequency.
- It can be built in a modular way and more levels can be added without changing the main circuit.

IET Power Electron., 2010, Vol. 3, Iss. 1, pp. 129–137
doi: 10.1049/iet-pel.2008.0253

• It provides several self-balanced voltage levels and only one driven switch, which make it ideal for feeding a diode clamped multilevel inverter.

The proposed circuit is based on the multilevel converters' principle, where each device blocks only one voltage level achieving high-voltage converters with low-voltage devices. The proposed converter is simulated and prototyped; experimental results prove the proposition's principle.

Future work will be done in the use of the MBC for balancing the DC link in the diode clamped multilevel inverter, especially for distributed generation applications based on multilevel converters.

9 References

[1] MIDDLEBROOK R.D.: 'Transformerless DC-to-DC converters with large conversion ratios', *IEEE Trans. Power Electron.*, 1988, **3**, (4), pp. 484–488

[2] MAKSIMOVIC D., CUK S.: 'Switching converters with wide DC conversion range', *IEEE Trans. Power Electron.*, 1991, **6**, (1), pp. 151–157

[3] AXELROD B., BERKOVICH Y., IOINOVICI A.: 'Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters', *IEEE Trans. Circuits Syst. I*, 2008, **55**, (2), pp. 687–696

[4] DONGYAN Z., PIETKIEWICZ A., CUK S.: 'A three-switch high-voltage converter', *IEEE Trans. Power Electron.*, 1999, **14**, (1), pp. 177–183

[5] ABUTBUL O., GHERLITZ A., BERKOVICH Y., IOINOVICI A.: 'Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit', *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, 2003, **50**, (8), pp. 1098–1102

[6] YONETANI S., KONDO Y., AKAGI H., FUJITA H.: 'A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: system design and experimentation of a 200-V 10-kVA laboratory model', *IEEE Trans. Ind. Appl.*, **44**, (2), pp. 672–680

[7] RODRIGUEZ J., LAI J.-S., PENG F.Z.: 'Multilevel inverters: a survey of topologies, controls, and applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 724–738

[8] LAI J.-S., PENG F.Z.: 'Multilevel converters – a new breed of power converters', *IEEE Trans. Ind. Appl.*, 1996, **32**, (3), pp. 509–517

[9] FAN Z., PENG F.Z., ZHAOMING Q.: 'Study of the multilevel converters in DC–DC applications'. IEEE 35th Annual Power Electronics Specialists Conf., PESC 04, 2004, vol. 2, pp. 1702–1706

[10] AXELROD B., BERKOVICH Y., IOINOVICI A.: 'A cascade boost-switched-capacitor-converter – two level inverter with an optimized multilevel output waveform', *IEEE Trans. Circuits Syst. I*, 2005, **52**, (12), pp. 2763–2770

[11] JULIO C.R.-C., RAMÍREZ J.M., PEDRO M.G.-V.: 'Novel DC–DC multilevel boost converter'. Proc. IEEE Power Electronics Specialists Conf., 2008

[12] IOINOVICI A.: 'Switched-capacitor power electronics circuits', *IEEE Circuits Syst. Mag.*, 2001, **1**, (3), pp. 37–42